JX2-CNT1

Version Update

from V. 2.11 to V. 3.01

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1.1   Version Updates - Survey

Version Updates - Survey			
Version	**Function**	**upgraded**	**corrected**
V. 3.01	Frequency Measurement	✓	
	Register 3xx3 "Status / Control of the Dual-Channel Counter"	✓	
	Reading in the SSI-Encoder		✓
V 2.11	Frequency Measurement	✓	
	Register 3xx8 "Filter Frequency"	✓	
	Master-Slave Operation	✓	
	Register 3xx3 "Status of the Dual-Channel Counter"	✓	

1.2   System Requirements

Software Versions of the Controllers and the JX6-SB(-I) Submodule	
Control	**Minimum Software Version**
JC-241, JC-243, JC-246, NANO-B, NANO-C, NANO-D	All Versions
JX6-SB(-I) (for JC-647, DELTA, JC-800)	All Versions

2   Expansions

2.1   Frequency Measurement

In register 3xx0 "Count Value / Frequency of the Dual-Channel Counter", up to now either the count value of the dual-channel counter or the frequency could be displayed. In order to make the count value and the frequency of the dual-channel counter readable, the frequency can from now on also be displayed via register 3xx7 "Parity Error Count". The time base will further be displayed in register 3xx1 "Offset / Time Base for Frequency Measuring of the Dual-Channel Counter".

For switching between the parity error count and the frequency value, bit 12 of register 3xx3 "Status / Control of the Dual-Channel Counter" is made use of. When bit 12 is set, the display set in register 3xx1 is simultaneously switched from offset to time base.

Switching between count value and frequency in register 3xx0 by means of bit 15 of register 3xx3 is still possible.

Register 3xx3 Bit 12 = 0 Register 3xx7: Parity Error Count	
Function	**Description**
Read	Actual parity error count
Write	New parity error count
Value range	-8,388,608 ... 8,388,607
Value after reset	0

Register 3xx3 Bit 12 = 1 Register 3xx7: Frequency of the Dual-Channel Counter	
Function	**Description**
Read	Actual frequency of the dual-channel counter
Write	Illegal
Value range	-8,388,608 ... 8,388,607 (increments / time base)
Value after reset	0

Please refer to the description of the frequency display in register 3xx0 in the document regarding the version update from version 2.09 to version 2.11.

2.2 Status / Control of the Dual-Channel Counter

Register 3xx3: Status / Control of the Dual-Channel Counter	
Function	**Description**
Read	Actual status, respectively control information
Write	Setting, respectively resetting, of bits 12 – 15 and resetting of bits 0, 4, and 6.
Value range	bit-coded, 24 bits
Value after reset	0

During writing, Bits 0, 4, and 6 are automatically reset, no matter, whether they had been pre-set for writing or not.

Meaning of the Individual Bits:

Bit 0:   **Strobed count value**

Bit 1:   **Reserved**

Bit 2:   **Reserved**

Bit 3:   **Counter set to zero**

Bit 4:   **Strobing value is overwritten**

Before resetting the latest strobing signal, the module has already received the next one.

Bit 5:   **Reserved**

Bit 6:   **Disturbance of the zero-crossings**

Either there is simultaneous changeover between K1 and K2, or else the counting frequence respectively speed is too high. The latter only occurs, if the input filter has been activated, see register 3xx8 "Filter Frequency".

Bit 7 - Bit 11:   **Reserved**

Bit 12*   **Activating, respectively deactivating, the frequency display via fegister 3xx7**

0 =   Display of the parity error count in register 3xx7
      Display of the dual-channel counter offset in register 3xx1

1 =   Display of the dual-channel counter frequency in register 3xx7
      Display of the time base for frequency measuring in register 3xx1

Bit 13:   **Reserved**

Meaning of the Individual Bits:

Bit 14:   **Selecting the master-slave operation**

0 =   Master-slave operation by JX2-SV1 or CAN-DIMA

1 =   Master-slave operation by JetMove 2xx

Bit 15:   **Activating, respectively deactivating, the frequency display via register 3xx0**

0 =   Display of the dual-channel counter value in register 3xx0
Display of the dual-channel counter offset in register 3xx1

1 =   Display of the dual-channel counter frequency in register 3xx0
Display of the time base for frequency measuring in register 3xx1

Bit 16 -   **Reserved**
Bit 23:

* new bits

3   Corrections

3.1   Reading in the SSI-Encoder

In the preceding software versions, SSI encoders of 10 bit or less cannot be read out properly. The problem is that sporadically the wrong encoder position has been read in.

As of this software version, this problem has been solved.

Important!

In connection with the JX2-CNT1 module, SSI encoders of less than 10 bit cannot be read in.